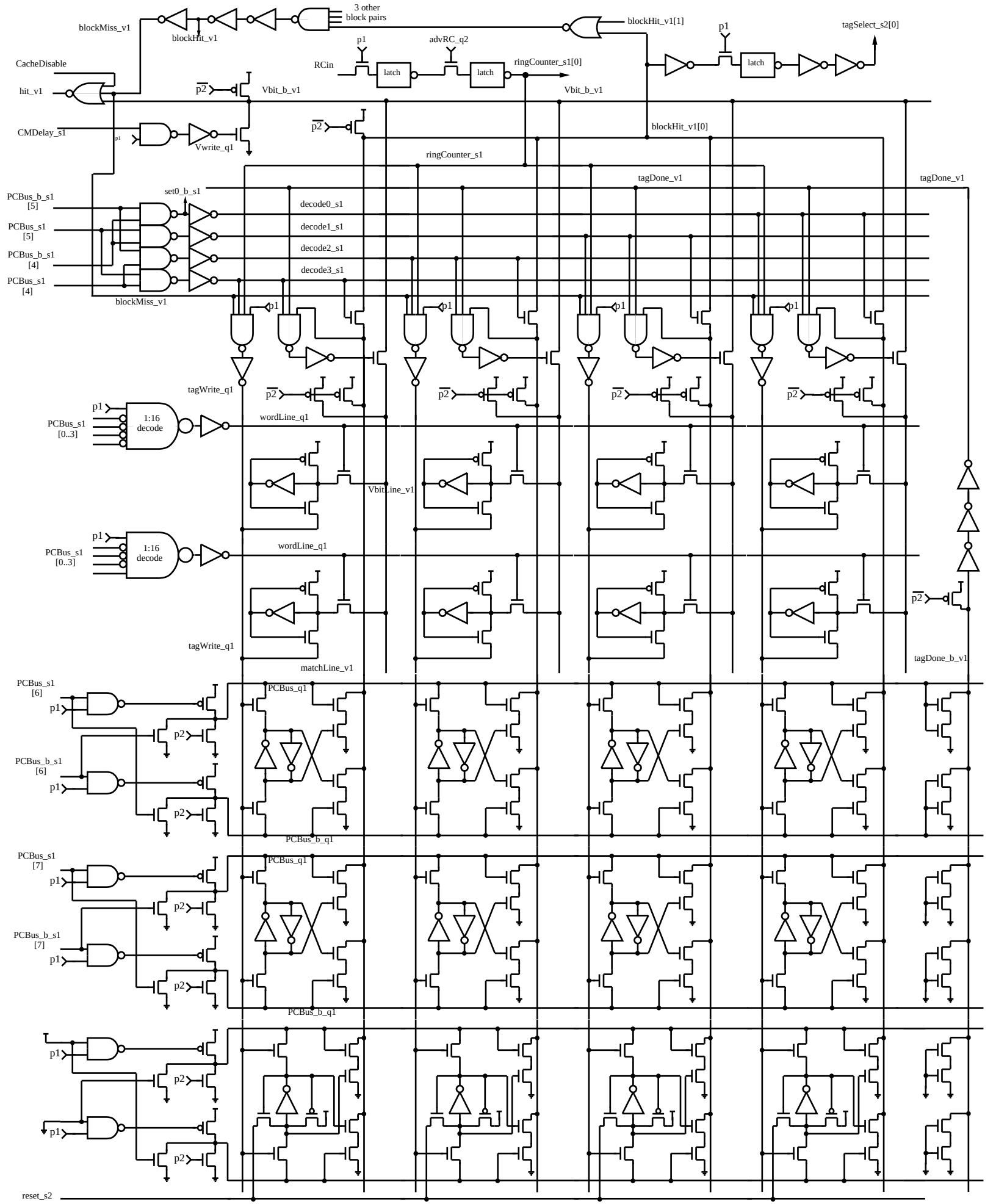
blockMiss_v1
blockHit_v1
3 other block pairs
blockHit_v1[1]
p1
tagSelect_s2[0]
CacheDisable
RCin
p1
advRC_q2
latch
latch
ringCounter_s1[0]
latch
hit_v1
p2
Vbit_b_v1
Vbit_b_v1
CMDelay_s1
p2
blockHit_v1[0]
Vwrite_q1
ringCounter_s1
tagDone_v1
tagDone_v1
set0_b_s1
PCBus_b_s1 [5]
PCBus_s1 [5]
PCBus_b_s1 [4]
PCBus_s1 [4]
decode0_s1
decode1_s1
decode2_s1
decode3_s1
blockMiss_v1
p1
tagWrite_q1
p2
p1
1:16 decode
PCBus_s1 [0..3]
wordLine_q1
VbitLine_v1
p1
1:16 decode
PCBus_s1 [0..3]
wordLine_q1
p2
tagWrite_q1
tagDone_b_v1
matchLine_v1
PCBus_s1 [6]
PCBus_q1
p1
p2
PCBus_b_s1 [6]
p1
p2
PCBus_b_q1
PCBus_s1 [7]
PCBus_q1
p1
p2
PCBus_b_s1 [7]
p1
p2
PCBus_b_q1
p1
p2
p1
p2
reset_s2